Overlay Metrology Results on Leading Edge Cu Processes

Vincent Vachellerie[a1], Délia Ristoiu [a2], Alain Deleporte[a3], Pierre-Olivier Sassoulas [a4], Philippe Spinelli [a5], Marc Poulingue[b6],Pascal Fabre[b7] Rolf Arendt[c8], Ganesh Sundaram[d9], Paul Knutrud[d10]

[a] STMicroelectronics, F-38926 Crolles Cedex, FRANCE

[b] Schlumberger Semiconductor Solutions Europe, 38170 Seyssinet – Pariset, FRANCE

[c] Schlumberger Semiconductor Solutions Europe, D-85737 Ismaning, GERMANY

[d] Schlumberger Semiconductor Solutions, Concord, MA 01742, USA

ABSTRACT

As geometrical dimensions of semiconductor devices decrease, the need to introduce Cu processes into the fabrication cycle becomes increasingly important as a means of maintaining line resistances and circuit time constants. However, the success of implementing such a fabrication process is dependent on the ability to characterize it through quantitative means, as such as Overlay metrology. In this paper we examine the overlay measurement results which have been obtained on a Cu based CMOS process at the 0.12um technology node. Overlay measurements were taken over a wide range of process conditions, and included wafers exhibiting extreme image contrast reversal, grainy conditions and low contrast. These factors have traditionally led to a decreased ability to make repeatable measurements, if the measurements could be made at all. Our results cover the important metrics of overlay metrology, and include precision, recipe portability, and measurement success rates. The results suggest that the overlay metrology issues encountered with such leading edge processes need not pose intractable barriers to obtaining reliable overlay metrology data.

Keywords: Overlay, Metrology, Cu, Alignment, Photolithography, Damascene

1. INTRODUCTION

Since the introduction of Cu processing, several studies have been conducted which have examined Overlay metrology issues [1]. This study in contrast concentrates on presenting the challenges to overlay measurements induced by state of the art processing. As such, we have been engaged in a study to characterize the Overlay registration metrology associated with a 0.12um Cu CMOS. Although the size of the Overlay target is not subject to the same dimensional constraints imposed upon CD targets, which scale with decreasing process technology nodes, and even if certain processes, such as damascene process lends itself well to being optical measured [4], the target measurement nonetheless present a metrology challenge [2]. These challenges are based on an ever-shrinking overlay budget that translates itself into a requirement for more precise overlay registration measurements [3], even as some new fabrication processes (new resist, BARC, ECD, CMP Copper,…) adversely modify the measurement targets.

2. EXPERIMENTAL AND MEASUREMENT METHODOLOGY

Since the backend overlay measurements represent a specific type of challenge, samples from back-end processes were chosen for this study. The 0.12um technology node wafers used in this investigation are marked by 11 measurement steps, of which 6 are considered critical in terms of overlay measurement. Cross sections of device structures are shown in Figure 1a,b, and c.

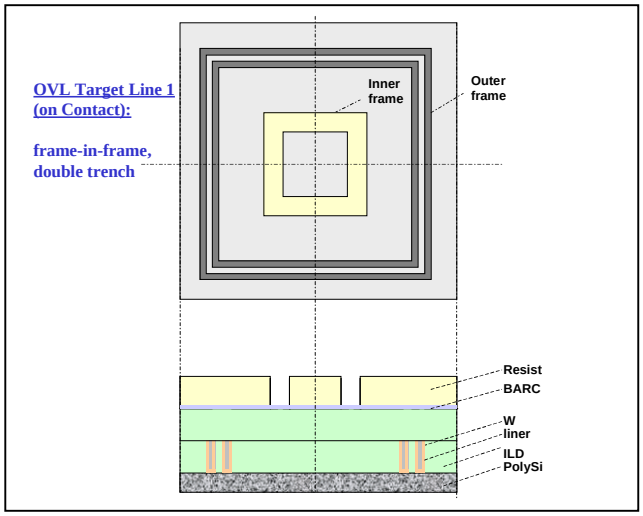


Figure 1a: line 1 overlay target design

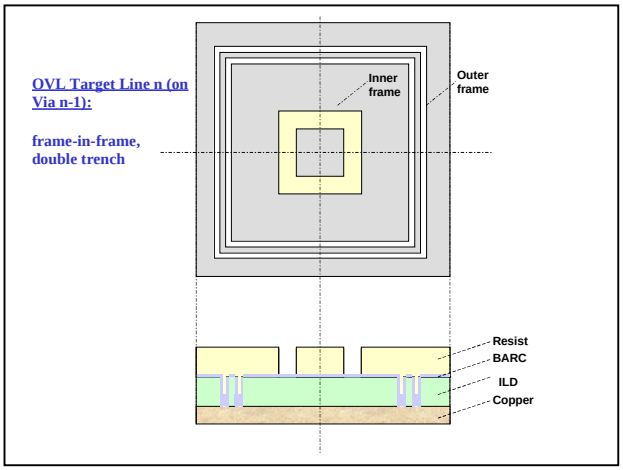


Figure 1b: line n on via n-1 target structure

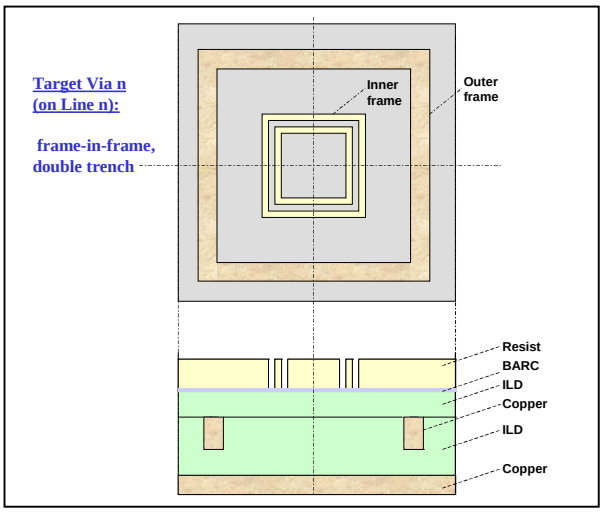


Figure 1c: via n on line n target structure

To characterize broadly the processing effects on overlay metrology, a wide variety of layers were selected for measurement (Table 1). Please note that the term metal and line are interchangeable.

Layer name	Critical layer	Reticules measured	Production lots measured
Line1	Yes	2	2
Via1	Yes	3	3
Line2	No	2	2
Via2	Yes	2	4
Line3	No	2	3
Via3	Yes	4	7
Line4	No	3	3
Via4	Yes	2	6
Line5	No	2	4
Via5	Yes	2	4
Line6	No	2	2

Table 1: Backend copper process layers, which were measured during this study. Number of reticules and production lots measured are displayed for each layer

The wafers were produced at STMicroelectronics Crolles using ASML /700 scanners and with 248nm resist. A Schlumberger IVS 135 Overlay Registration and CD metrology system was used for the overlay measurements. Measurement precision, system matching and measurement success rates were studied as a function of layer, as these metrics were determined to be most affected by the processing technology. Overall, 11 copper backend layers on 0.12um technology were measured.

Precision measurements entailed the measurement of 2 wafers per lot (a third different one is used to create and optimize the recipe), with 12 dies per wafer, and 4 sites per die, which correspond to production level measurement plans. Iterative optimization routines were employed to create wide process-latitude measurement recipes. These recipes were optimized to accommodate layers exhibiting extremely wide process variations, without requiring adjustment.

In order to save time for recipe creation, experiments have been performed to define a strategy for TIS calibration. Thus, a calibration file was generated at the time of recipe creation in order to compensate for TIS. The calibrated TIS provided a measure of how well the calibration file models the actual TIS measured on a wafer. The sampling plan chosen for production purposes is 5 fields spread on the wafer surface, 4 sites per field.

After checking the impact of the number of measurement repeats on precision (figure 2), we chose to measure wafers 3 times dynamically in order to get statistics data (standard deviation, average, minimum, maximum values), while saving time during recipe creation.

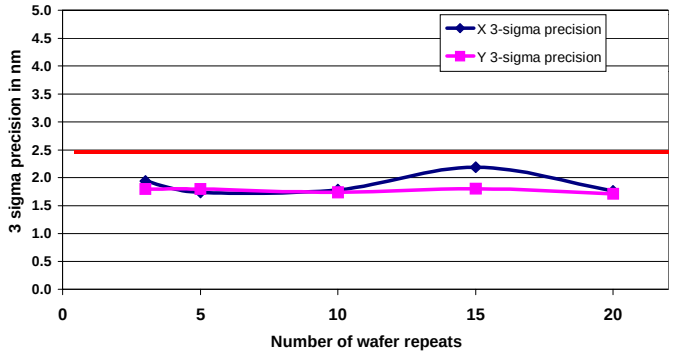


Figure 2: impact of the number of measurement repeats on 3-sigma precision

It should be noted that these tests were conducted in R&D Logic semiconductor plant where more than 1 device is introduced per day. As such, one has to be able to generate thousands of recipes with adequate performance. This is currently achieved with an “off-line recipe creator” software package, which allows

all recipes for new devices to be generated without being in front of the tool with a wafer. This capability saves cycle time, equipment time and human resources - i.e. it increases overall productivity. These new recipes are generated offline from “golden recipes”. Golden recipes are created and optimized with a wafer in front of the overlay tool for each layer. The challenge for golden recipes is that, on top of “within wafer”, “wafer-to-wafer” or “lot-to-lot” process variation, they will have to cope with “device-to-device” process variation (induced by pattern density differences). Therefore, the goal is not only to get good performance on the device used to create the golden recipe, but also to be able to maintain it on the other devices, that will be measured using off-line created recipes. This is a key point in speeding up the technology learning curve. During this study we have used the Remote Job Generator (RJG) software package which is designed to create off-line recipes for IVS135.

3. RESULTS AND DISCUSSION

3.1 Process Induced Contrast Variation

3.1.a. wafer alignment

Fundamental to the successful measurement of overlay targets are the steps leading to the actual measurement itself. These steps typically entail the initial location of reference (wafer alignment feature) points through a pattern recognition scheme. In addition, in order to improve the benefit of the off-line recipe creator, wafer alignment features are usually set to be identical in the scribe line in terms of design and position. So that, for one layer, the same reference images will be useable for every device. Only the position of these features will change within the wafer.
Current state of the art process can lead to image variations of the alignment points across the wafer, from wafer to wafer, from lot to lot or device to device, leading ultimately to an inability to measure the target, as pattern recognition algorithms will fail to identify the feature from the reference image. This translate itself into cycle time increase and working time. Thickness non-uniformity or abnormal presence of residues often causes these image variations.
An example of this type of process related metrology issue is shown in Figure 2, below.

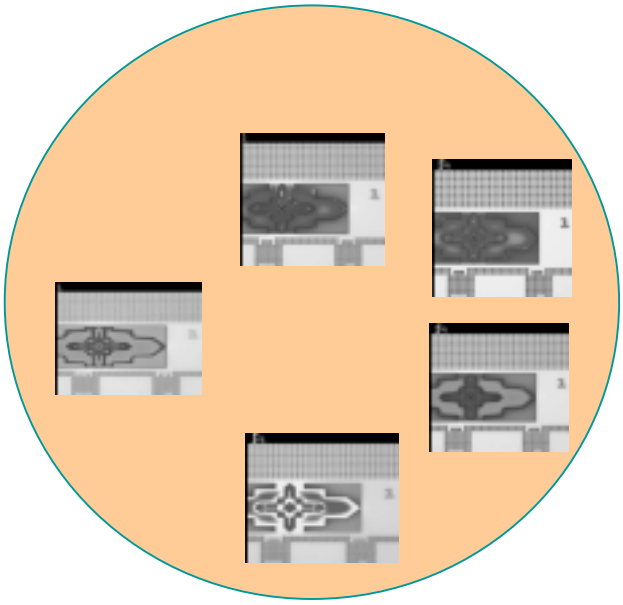


Figure 2. Reference point image variations seen across wafer can present major challenges to measurement

A substantial process challenge lies in making the wafer alignment feature insensitive to process variation. Therefore, good wafer alignment capability gives more flexibility for metrology users. IVS135 offers

several means of addressing the alignment issues including an adjustable pattern recognition area and enhanced algorithms to deal successfully with contrast variations.
Table 2 provides a summary of the pattern recognition success rate obtained on the metrology measurement system by optimizing the pattern recognition to deal with a wide set of image variation. These success rates of 99-100% are the key in moving the measurement process to the next step – namely the repeatable measurement of the registration target.

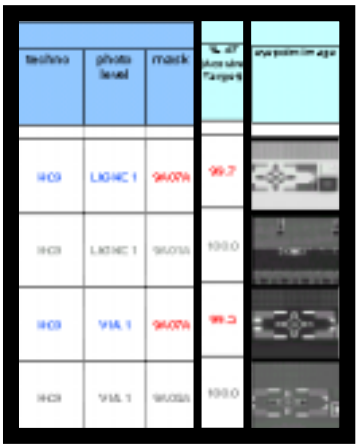
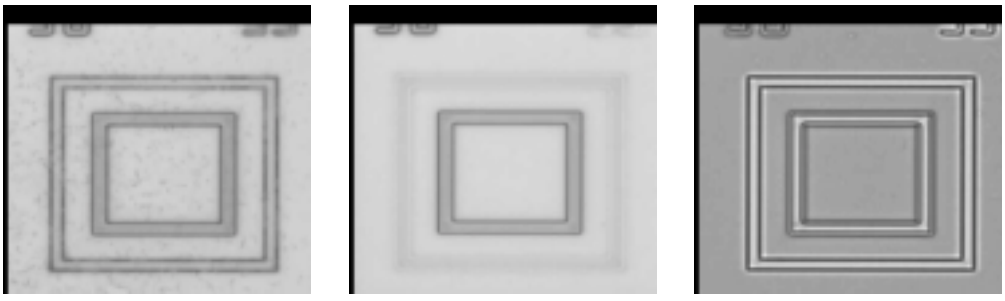


Table 2. High pattern recognition acquisition rate is required for measurement

3.1.b. overlay target

The measurement of the overlay targets poses similar challenges to that seen in at the reference feature location step. These process-induced variations produce targets which vary in image quality and intensity. These variations are causes by either thickness non-uniformity across the wafer or from wafer to wafer, lot to lot, device to device, or scanner focus conditions, or copper residues after CMP (on Via/line overlay targets).
To avoid these non-desirable effects, one could change the target design or its stack. However, this is not particularly easy since such changes must be done with the constraint that WIS [Wafer Induced Shift] effects are minimized and optical visibility is maintained. However, when the target design change is not practical then the capability of the measurement tool must be sufficient to cope with these process effects and maintain strong target acquisition success rate and precision. The system ability to accommodate these process effects are made easier by the inclusion of features such as adjustable pattern recognition area, adjustable focus area, focus option, degrain algorithm, strong pattern recognition algorithm, ….
Examples of typical process induced contrast variation at the line4 layer is shown in Figure 4 a,b,c.



a/ lot 1 recipe a b/ lot 2 recipe a c/ lot 2: recipe a optimized

Figure 4: Line 4 overlay targets for two production lots 1 & 2. Pictures a & b describe contrast variations observed between lots 1 & 2. Picture c describes contrast enhancement obtained after recipe optimization.

Figure 4 shows an example of contrast variation between two production lots at the same layer and describes the results obtained before and after optimizing the recipe. The step height variations between

inner and outer frames come from thickness non-uniformity. The slope variation on the inner frame is caused by the scanner focus changes. With the optimized recipe with enhanced contrast, process-induced changes are dealt with by the metrology system's ability to adapt to different contrast and focus conditions. The results again show very good 3 sigma precision on overlay measurements (table 3):

Lot name	Layer	Job plan	3σ x overlay precision (nm)	3σ y overlay precision (nm)
1	Line 4	original recipe	0.99	1.23
2	Line 4	original recipe	3.9	>20
2	Line 4	optimized recipe	2.1	2.1

Table 3: summary of 3 sigma precision obtained for the lot 1 & 2 before and after recipe optimization to compensate for contrast variation from lot 1 & 2

3.2 Challenges of Non-symmetric Overlay target edges

An additional problem encountered by the overlay measurement tool is the process induced target asymmetry, which leads to overlay accuracy errors. This can be causes can be either:

- Voids or dishing after metal deposition (W or Copper), CMP. This is evident on Via/Line overlay targets or Line1/CT(contact).
- BARC (anti reflection coating) depletion, which induces a parasitic signal on the edge of the line as we look at it optically, and therefore leads to target asymmetry. It can be seen on Line/Via overlay targets.
- Slope and CD variation on resist caused by focus/exposure conditions. This can be seen especially on Via/Line overlay targets.

Target asymmetry problems however do lend themselves to be solved by redesign efforts. Such redesign solutions can be in the form of "double trench" target design or "segmented" target as shown in figure 5 a,b,c. Such redesign targets are more in line with those seen in the production settings.

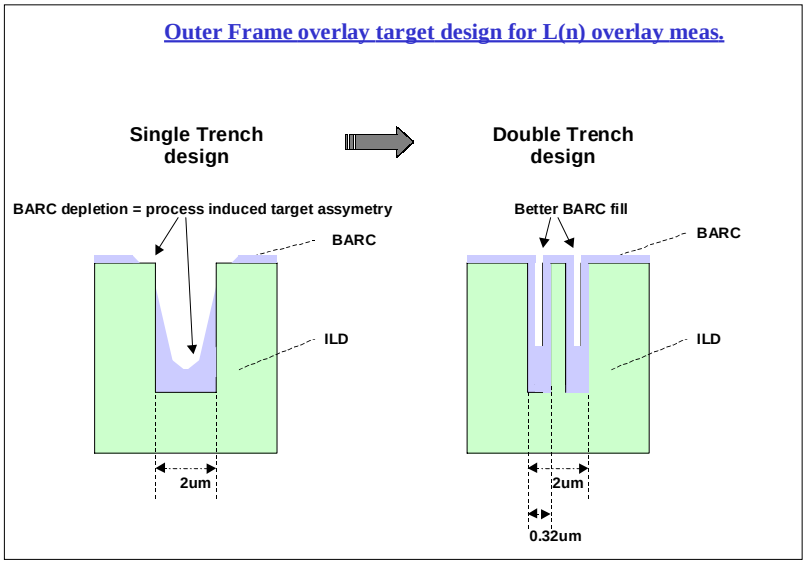


Figure 5a: sketches displaying single and double trench designs used for the outer frame of an overlay Line over Via target (single damascene process)

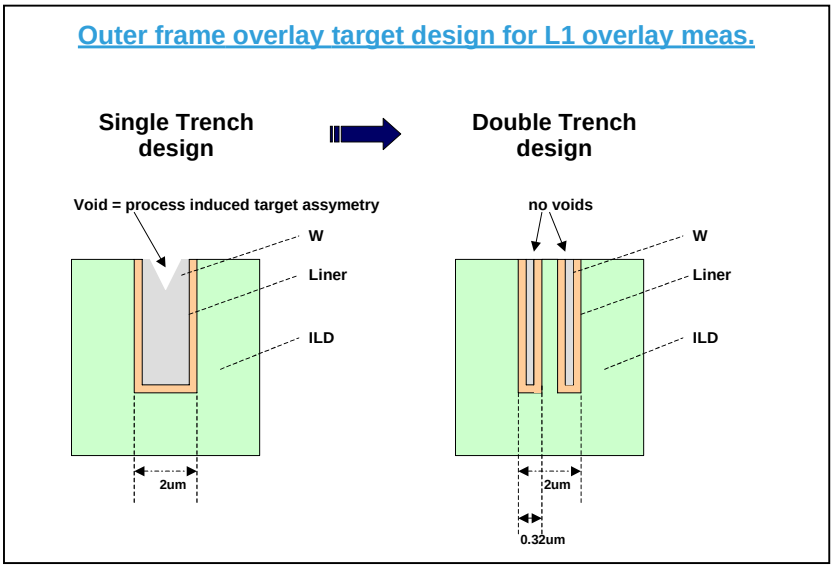


Figure 5b: sketches displaying single and double trench designs used for the outer frame of an overlay Line 1 over Contact target (filled with W)

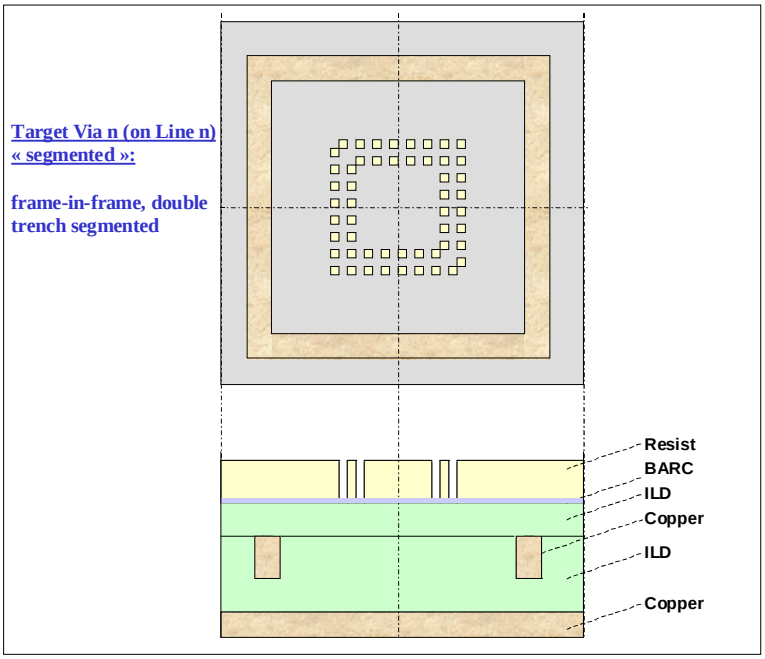


Figure 5c: sketch showing the new design used for via over line overlay target. Inner frame consist of a double trench of dense via holes forming lines

Non-symmetrical effects are depicted in Figure 6a and 6b, which consists of non-symmetric edges for Via 1 layer targets. This is due to a slope variation on resist, caused by stepper focus exposure conditions. This non-symmetry was generating fliers in the measurement data.. Working on the recipe we found that with another focus method and offset we were able to eliminate these fliers and obtain good measurement success rate.

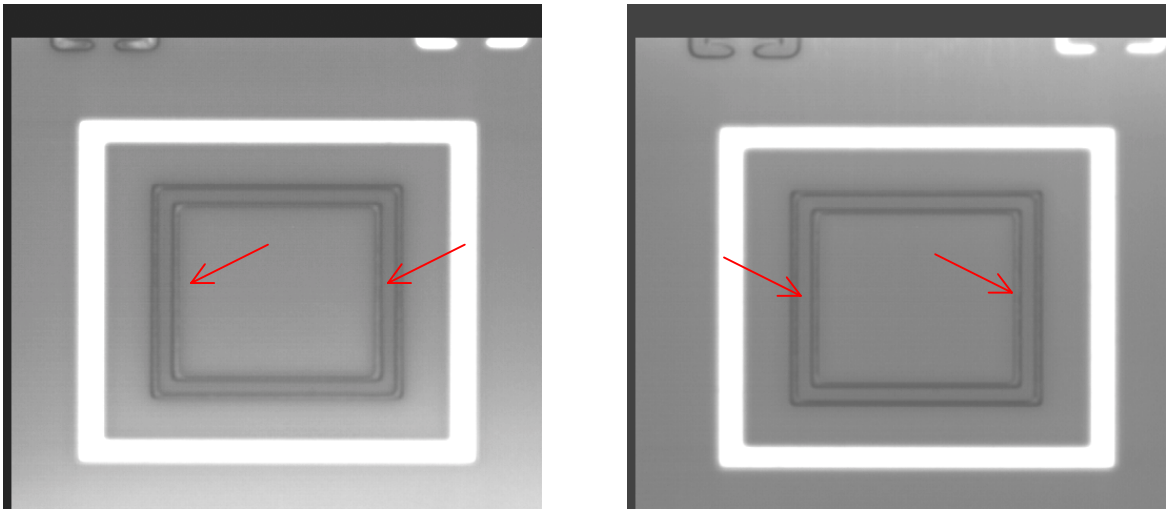
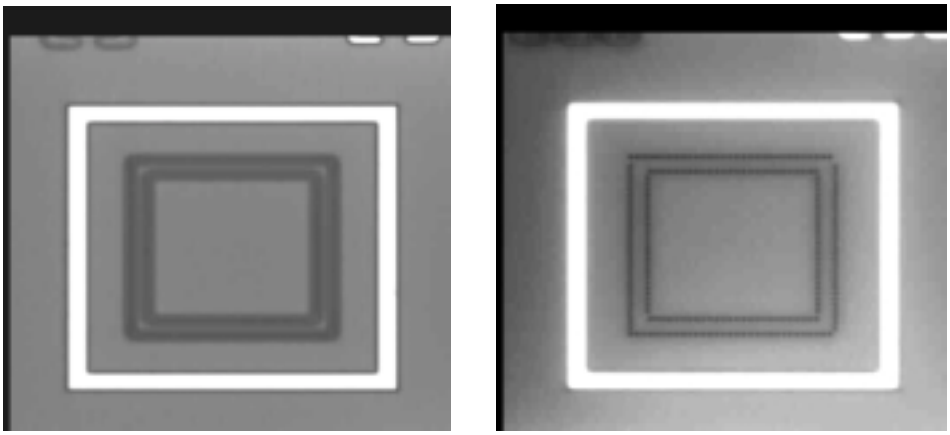


Figure 6: via 1 level overlay target showing non-symmetric edges for inner box as pointed out with red arrows

New reticules with classical and "segmented" registration targets (figure 5 c) on via 1 level have been tested (see figure 7). The inner frame of the "segmented" target is made of a double trench of via holes line as you can see clearly on figure 7b. The "segmented" target exhibits a sharper image than the classical target. First overlay measurements, performed with the recipe created with classical target, show good 3-sigma precision below 4 nm (table 4). A new recipe using this new design target has been created and optimized. Very good 3-sigma precision has been obtained: below 2 nm in x direction and below 2.5 nm in y direction (table 4). These precision values are in the same range than those obtained with the classical target (table4). As the "segmented" target shows sharper image and is made with the same design as the product itself, the recipe robustness should be improved.



a/classical V1 target b/ new design V1 target

Figure 7 a/ & b/: picture a/ show a classical V1 layer overlay target and picture b/ the new design target on the same wafer with "segmented" inner box.

level	target	lot	recipe	3 σ x (nm)	3 σy (nm)	Measurement success rate %
V1	segmented	A	Recipe created with classical target	3.74	3.36	100
V1	segmented	A	New recipe created & optimized with segmented target	1.86	2.49	100
V1	classical	average	Recipe created with classical target Average values obtained during this study	1.49	1.84	99

Table 4 : overlay precision and target acquisition obtained on V1 "segmented" registration target compared with the average values measured on the different V1 lots

As a conclusion to this section, it appears that in going to smaller technology nodes, the differences between overlay target design and product design rules are increasing. As a result when target design is far removed from the process rules, non-linear and asymmetrical effects are exacerbated.

3.3 Process Induced Edge Profile variation (grainy metals)

Another challenge encountered by the measurement process is the edge profile variation that arises with processes that produce grainy metals. Wafers that use W-CMP process in conjunction with Al/Cu processes (first Metal layer) exhibit edge variations within a wafer, linked to the graininess of the metal. This will lead to poor precision and measurement inaccuracy.
Figure 8 and 9 describes the problem and the means used to overcome it.

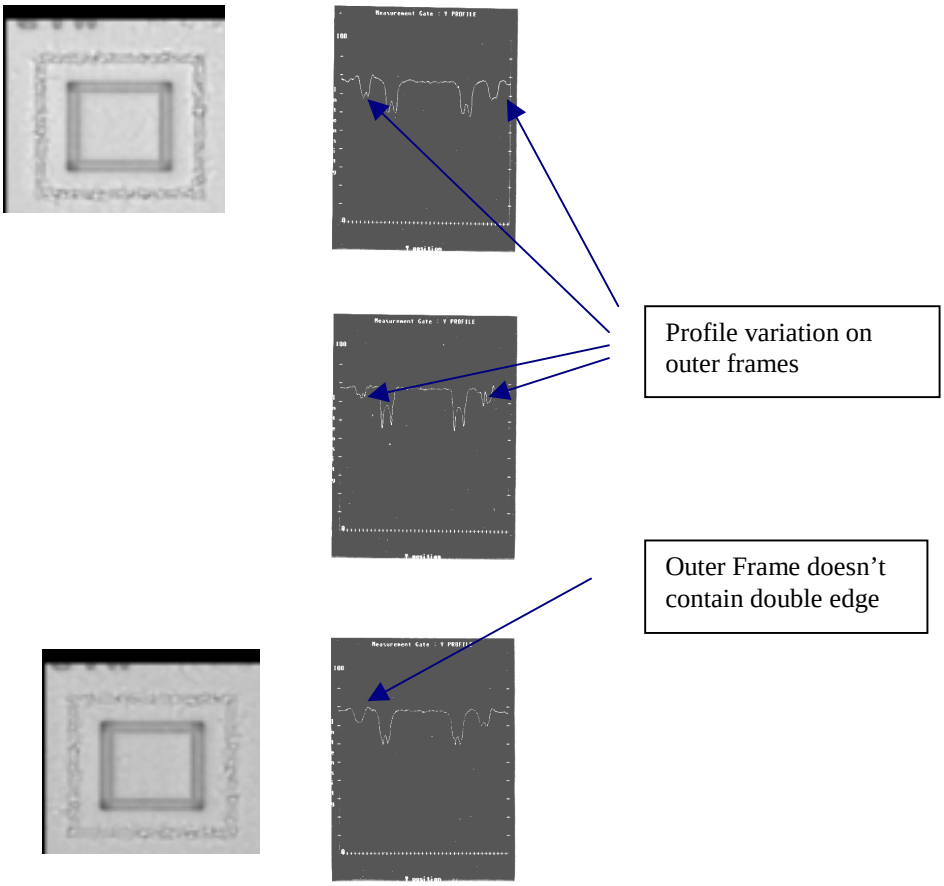


Figure 8.

Profile variations due to the grainy aspect of the overlay target (as described in figure 9) can decrease the 3 sigma precision and the measurement success rate. On the metal layer described in figure 8, measurement success rate decreases to 62.5% (see table 5). Using the degrain algorithm we reach back measurement success rate up to 99% with good 3 sigma measurement precision below 3 nm (table 5).

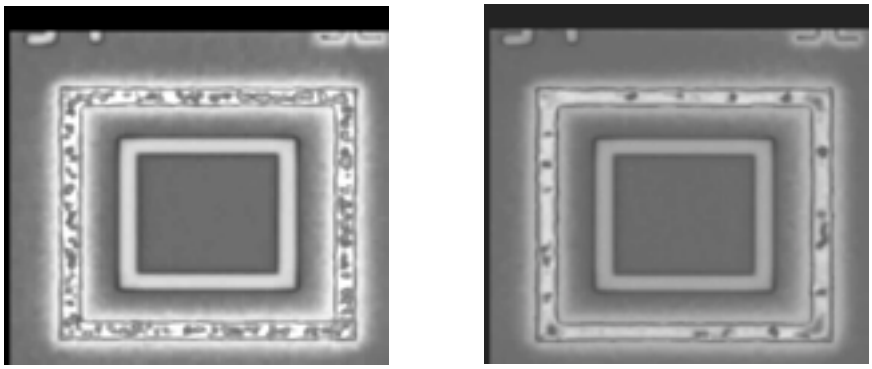


Figure 9: metal layer overlay targets with grainy surface due to CMP metal process

	Degrain algorithm	**3 sigma x precision (nm)**	**3 sigma y precision (nm)**	**measurement success rate %**
Original recipe	Off	3.28	3.4	62.5
Optimized recipe	On	2.91	2.87	99.8

Table 5: 3 sigma precision and measurement success rate obtained on grainy metal registration targets with and without degrain algorithm.

3.4 Overlay Metrics

The measurements metrics which are generally noted in Overlay registration include, most importantly, the precision, the measurement success rates, and the system matching. Table 6a & Table 6b provide the full spectrum of parameters measured during the course of the study and the values obtained. Results displayed were obtained both from recipes created on the overlay tool and with the offline recipe creator.

	overlay measurement statistic in nm for x & y directions						
	3 sigma x values	3 sigma y values	max x	max y	min x	min y	lot nb
global	1.61	1.62	3.09	2.81	0.69	0.90	40
line1	2.06	1.52	2.20	1.55	1.92	1.49	2
line2	1.75	2.06	2.24	2.81	1.27	1.30	2
line3	1.54	1.66	1.72	1.98	1.31	1.44	3
line4	1.48	1.74	2.02	2.10	0.99	1.23	3
line5	1.46	1.52	1.66	1.73	1.24	1.40	4
line6	1.36	1.52	2.03	2.02	0.69	1.01	2
via1	1.49	1.84	2.20	2.65	0.78	1.19	3
via2	1.30	1.32	1.41	1.62	1.15	1.13	4
via3	1.80	2.05	3.09	2.71	1.11	1.30	7
via4	2.12	1.44	2.75	1.93	1.33	0.90	6
via5	1.04	1.12	1.09	1.13	1.02	1.11	4

Table 6a: summary of the statistics results obtained during this study.3 sigma precision, maximum & minimum overlay values and standard deviation of the 3sigma precision are displayed for each layer and the average of all measured layers

	calibrated tis (nm)		Measurement success rate %		Tool to tool matching (nm)		
	Mean cal tisx	Mean cal tisy	average value	Minimum value	Delta between the mean overlay values	Delta between the mean overlay values	Lots measured
global	0.12	0.09	99.66	95.49			40
line1	0.36	0.90	99.83	99.65			2
line2	0.77	-0.71	100.00	100.00	0.9	1.89	2
line3	-0.64	0.52	97.57	95.49			3
line4	0.02	-0.07	99.31	98.61			3
line5	-0.32	-0.12	99.83	99.65			4
line6	-0.07	-0.36	100.00	100.00			2
via1	0.17	1.04	99.65	99.29	0.28	1.87	3
via2	0.22	-0.79	99.88	99.65			4
via3	0.94	0.15	99.85	98.96			7
via4	0.03	0.22	99.94	99.65			6
via5	-0.41	0.21	99.91	99.65			4

Table 6b: Calibrated Tis, measurement success rate and tool to tool matching results obtained during this study. Tool to tool matching has been performed on the same wafer with same recipe on two Schlumberger IVS 135 Overlay Registration and CD metrology system.

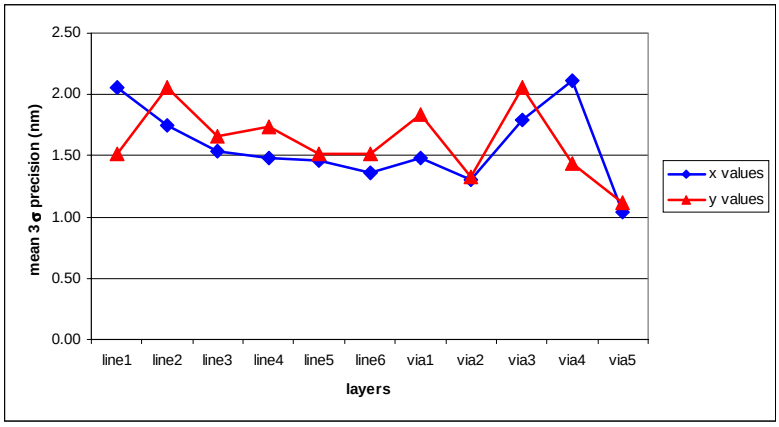


Figure 11: Graph showing 3 sigma precision obtained for each measured layer

The results show excellent precision, calibrated TIS, measurement success rates, and system matching even under the most adverse conditions. Mean values for the data are shown. The data set shown has not been filtered to cull data. The layer chosen for the matching work was selected for its difficulty. Matching was accomplished by running exactly the same recipe on two different overlay measurement systems, measuring the same wafer. Based on the data a few observations can be made. The data clearly indicates that leading edge Cu processes pose significant challenges, but that these can be overcome with flexible and adaptive measurement and pattern recognition algorithms. Additionally, the precision and matching values obtained show that the ITRS roadmap for overlay metrology requirements for the 120nm process node can be satisfied easily (ITRS2001: Precision (3sigma) including Tool Matching < 4.2nm, assuming a process tolerance of 10%)

3.5 Data Filtering

A common but serious problem that can be encountered as a result of adverse processing is that of data excursion - excursions which exceed the expected deviations for the process. The causes can either be an abnormal photo process on the target, or a mask issue, recipe error, focus or illumination failure….

A go/no go control is often done on min/max overlay values over a lot. This means that, if an excursion occurs, the lot will be stopped and will require some analysis, leading to cycle time increase and time spent for analysis. The inclusion of such data in the overall data set can also lead to incorrect adjustment information for the lithography system and especially in case of automatic feedback to scanner.

As a result it is of value at times to apply carefully and judiciously, data filters to remove obvious data fliers. An example of the filtering process using the Metroboost Overlay Booster software is shown in Figure 10.

The cutoff filter will remove all the measurement points having overlay values greater than a chosen threshold. This threshold will be adjusted taking into account the process capability. In our study we have chosen a value of 350 nm (see figure 12). The number of removed measurement points is noted. If this number is too high, wafer measurements will not be validated and no feedback analysis file will be generated.

Sigma residual filter is another filter that can be used. This filter will remove measurement points that are not fitting well with the overlay analysis model. The residual sigma, which describes how well measurements are fitting with the overlay model, is correlated with the distribution of measurement points and the number of fliers. Such a filter must be used with care.

A good solution is to associate both cut off and sigma residual filters. Parameters have been adjusted in order not to remove accurate measurement points. We have chosen a 2.8 sigma residual filter. After the application of the sigma residual filter it was noted that an extra 2 to 3 points were removed beyond those taking out by the cut off filter.

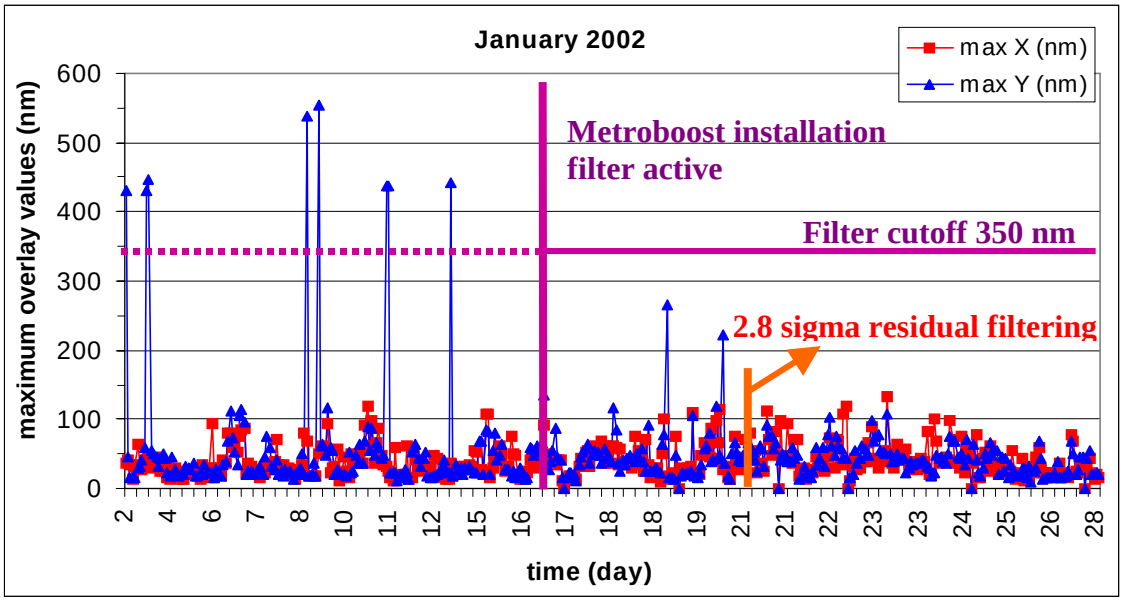


Figure 12. Filtering of Obvious data fliers to prevent skewing of remaining data set

mask	level	lot	Nb of pts measured	Nb of "good points" (without flyers)	remaining points after filtering (2.8sigma on residuals + 350nm cutoff)
A	V4	1	90	89	86
		2	81	78	78
		3	84	79	79
		4	66	61	61
		5	61	50	49
		6	78	73	73
	L1	10	89	84	84
		11	85	84	81
		12	81	80	78
		13	80	75	74
		14	94	91	89
		15	96	96	94
	L5	16	96	79	76
B	V1	7	94	94	81
C	L4	8	55	48	48
		9	67	65	65

Table 7: summary of results obtained after simulation 350nm cut-off filter and 2.8 sigma residual filtering on measurement data files for different level and production lots.

4. CONCLUSIONS

Through this study we have been able to demonstrate the types of overlay metrology issues that arise as a result of leading edge Cu processes. We have also shown the tool set and methodology we have used to overcome these problems, and establish capability in performing repeatable overlay measurements at the 0.12um process node. This work is now being extended to qualified the 0.10 µm node process. It appears that future work on overlay, based on optical techniques, will concentrate on new target design closer to the product design rules in order to avoid process induced effects, and measurement tool capabilities and flexibility to be able to cope with these effects (algorithms,…).

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Contact Author Information :

Vincent Vachellerie, STMicroelectronics, 850 rue Jean Monnet , 38926 Crolles cedex France, vincent.vachellerie@st.com, phone : 011 (33) 476925001, fax 011 (33) 476089825

Ganesh Sundaram, Schlumberger Semiconductor Solutions, 45 Winthrop street, Concord, MA 01742, USA, gsundaram@slb.com, phone : (978) 318 4014, fax : (978) 369 0850

Marc Poulingue, Schlumberger Semiconductor Solutions Europe, 18 rue de la Tuilerie, 38170 Seyssinet-Pariset – France, poulingue@montrouge.tt.slb.com, phone 011 (33) 620171569, fax 011 (33) 476703054