

Algorithm Implementation and Techniques for Providing More Reliable Overlay Measurements and Better Tracking of the Shallow Trench Isolation (STI) Process

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ABSTRACT

The intent of Chemical Mechanical Polishing (CMP) is to minimize topography across a wafer. Topography is essential for edge contrast in optical overlay metrology¹. Many of the advanced CMP processes cause a reduction in step height to much less than 20 Angstroms². Conventional Overlay Metrology measurement optics require step heights in excess of 50 Angstroms to provide sufficient signal and contrast for algorithms to function properly. CMP further complicates the measurement task by causing significant step height and film thickness (contrast) variations as well as introducing asymmetry across a single overlay measurement target³. Such targets can be difficult to measure in standard metal and contact CMP applications let alone more modern front end CMP processes like Shallow Trench Isolation (STI). The registration marks become much more difficult to observe. Robust broadband optics with spatial filtering improves the contrast of the image; but the granularity of the substrate, the variation in edge detail, and the asymmetry of the registration mark can overwhelm a standard measurement algorithm. The registration mark measurement precision, accuracy and success rate can suffer due to the process variation in an aggressive front end CMP application such as STI.

This paper presents the results of a new algorithm designed to improve the success rate, precision and accuracy of the measurements for low contrast targets produced by STI. The paper will also review the algorithm and discuss the results of target design optimization. Results will be provided from multiple lots with multiple wafer analyses demonstrating the effectiveness of the algorithm. Measurement yields improve from the 35% - 50% success rate using current algorithms to 99% - 100% success rate using the new algorithm. Precision was improved from 10nm to 3nm, and as low as 1.2 nanometers 3σ . The true success of the algorithm is not just the improved measurement success, precision and accuracy; but it is in the verification that the edges are detected and measured accurately. Many current algorithms are giving estimates.

1. INTRODUCTION

Advances in process and design are required parts of each new generation of DRAM chips. Many challenges are presented by these advances. One of the significant challenges facing the industry today is being able to optically measure overlay registration after front end CMP processes. The CMP process can leave the surface of the wafer so flat that when later films are deposited it is virtually impossible to see any topography. And, if the film is opaque, it is impossible to see through the film at the features buried below.

In cases like this, a work around is required to be able to measure overlay. The work around includes extra processing steps which rob the company of much of the financial benefit from the new processes and designs. The development of an optical overlay measuring tool that can see the faint edges left after front end CMP processes is key to realizing all the benefits that come from advancing the process and technology in manufacturing.

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2. STI VERSUS LOCOS

DRAM memory requires electrical isolation between the silicon active areas of each memory cell. In the LOCOS (Local Oxidation Of Silicon) process the electrical separation was accomplished by growing a thick oxide in the isolation area. Growing a thick oxide creates a profile with a slope up on one side, a small 'plateau' of thick oxide in the middle, and then a slope back down the other side to the silicon. The space that is wasted is the area where the oxide is too thick to be an active part of the memory cell and too thin to be part of the isolation mechanism. It has no function in the DRAM memory cell and yet exists around every single cell, see Figure 1.

The STI process allows the overall chip size to be shrunk by eliminating wasted space around each cell. By cutting a trench down into the wafer and filling it with oxide the STI process creates a profile where there is no oxide, then a thick oxide, and then no oxide on the other side. The step down into the trench replaces the sloped areas on each side of the LOCOS thick oxide; eliminating the wasted space allowing cells to be placed tighter together. The challenge in the STI process is it requires a Chemical Mechanical Polish (CMP) step. The uniformity of the CMP process can be difficult to control, yet directly impacts the quality of the edges necessary to analyze the overlay. The small step height left remaining in the oxide can also present other challenges at later levels if opaque films are used. The combination of low topography and the fact that you can not see down through the opaque film to see the edge of the silicon trench results in very low signal to noise ratio for optical overlay measurement tools.

LOCOS

In this process a nitride film is deposited on the wafer on top of a thin oxide buffer film. The nitride is then patterned and etched out of the isolation areas and is left in the active cell area. The nitride is then used as a local block to the oxidation of the silicon in a high temp, high humidity, diffusion furnace process. A thick oxide grows in the areas not covered by silicon. The oxygen diffuses from the oxide surface down to the silicon interface where it reacts with the silicon to form SiO_2 . This Adds bulk so the oxide forms a big bump. Once the oxide has grown the diffusion of the oxygen through the film happens vertically and horizontally. Oxidation in the vertical direction is desired. Oxidation in the horizontal direction is not desired. This results in some growth under the edge of the nitride and in fact the nitride is pushed up at the edges. This is where the sloped region on both sides of the resulting profile is formed. This area is often referred to as the 'Birds Beak' region, see Figure 1.

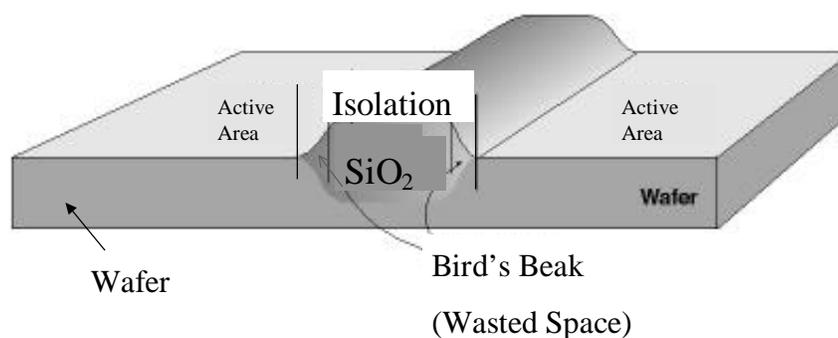


Figure 1 'Birds Beak', LOCOS Cross-section

STI

In this process a trench is etched down into the silicon of the wafer. A deposited oxide film is then put down thick enough that it more than fills the trench. A CMP is then used to remove the oxide off the horizontal surfaces and leave the trench filled. This is a very critical step for the process because the CMP removes oxide off the active areas, see Figure 2. The memory cell is very sensitive to any scratches or other silicon damage in this area. Yield loss from CMP problems at this point in the process can be very high.

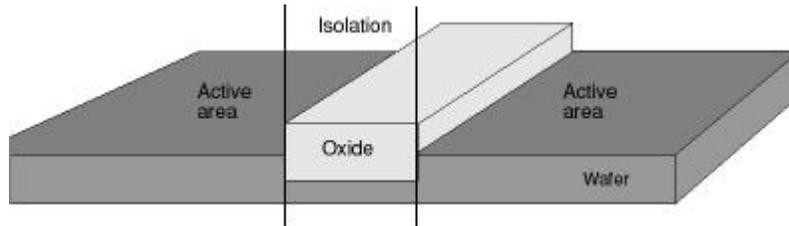


Figure 2 STI, CMP Cross-section

The concept is easy. Dealing with the impact of the CMP step in the process is the challenge.

3. SEVEN PROCESS STEPS - THE PREVIOUS METHOD

Levels following CMP steps can be challenging, especially if that level has an opaque film deposited on the wafer. The CMP step leaves the wafer surface very smooth. The opaque film acts like a mirror. It prevents optical systems from 'looking' down through the film and 'seeing' the topography from the previous patterns. This combination can prevent optical overlay metrology tools from functioning, or worse yet it contributes to added alignment uncertainty and potential yield loss. The short term solution has been to pattern and etch the material off the registration targets before the Photo steps for that level.

This patterning and etching involves seven extra process steps. An extra reticle is required as well. The seven steps are:

- 1) Prime
- 2) Coat
- 3) Expose
- 4) Develop
- 5) Etch
- 6) Dry Strip
- 7) Piranha (wet clean or strip)

Extra process steps take time and cost money. An overlay tool capable of measuring After Develop Inspect (ADI) registration is required to avoid these extra steps. Such a tool can provide significant cost and time savings with the elimination of these seven steps.

4. STI METROLOGY CHALLENGES

Current techniques for edge detection and edge locations do not work on a production basis. Measurement success rates can fall far below 50% of the sites analyzed. The edge detection begins to fail affecting accuracy as well as precision. A new algorithm was specifically designed to account for the variable and low optical contrast, and to accommodate the lithography from the STI process. The standard algorithm has been modified to accommodate the low contrast and site to site variations that are typical of the STI and other front end CMP processes. This provides the user with the freedom of not letting the metrology requirement dictate changes in the process and flexibility and in choosing registration features. It provides the customer more flexibility in the processing of production wafers without requiring additional production or measurement steps, or sacrificing measurement success rates, accuracy, or precision.

A standard optical image of the STI process has so little contrast that the edges are at times invisible to the eye and to the metrology tool, see Figure 3. Optical spatial filtering and normalization creates much more contrast as seen in Figure 4. The STI process does not provide uniform or high contrast optical images, as seen in unfiltered normalized images in Figure 5 and Figure 6. Variability from site to site created by subtle changes in the oxide thickness prove difficult. The increased granularity that is produced by spatial filtering may also be problematic, see Figure 7 and Figure 8. The interference from these variations will be negated and accuracy and precision will be enhanced if the algorithm accounts for the variation at all edges of the inner and outer features. The noise peak to background ratio will vary greatly. The ratio of edge peaks will also change and shift measurements to different set of lines. Such “false” measurements appear to be correct, and are typical of most basic algorithms.

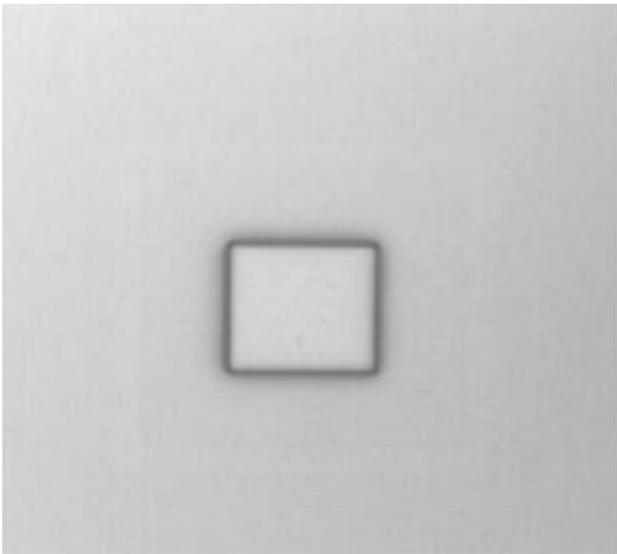


Figure 3. Unfiltered optical image of STI process

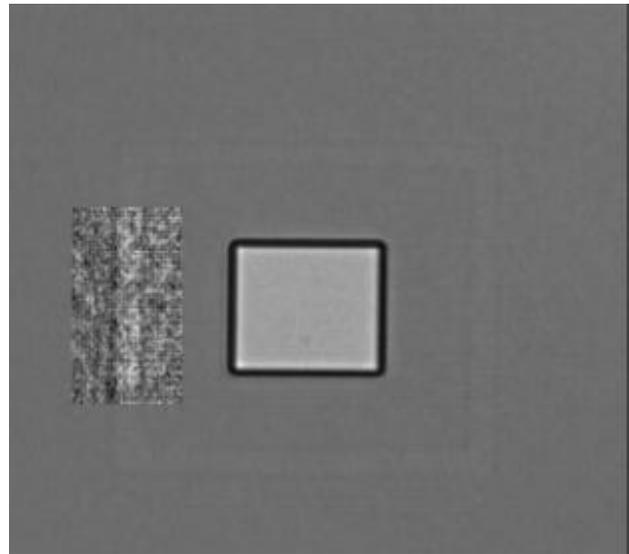


Figure 4. Filtered/Normalized optical image of STI Process.

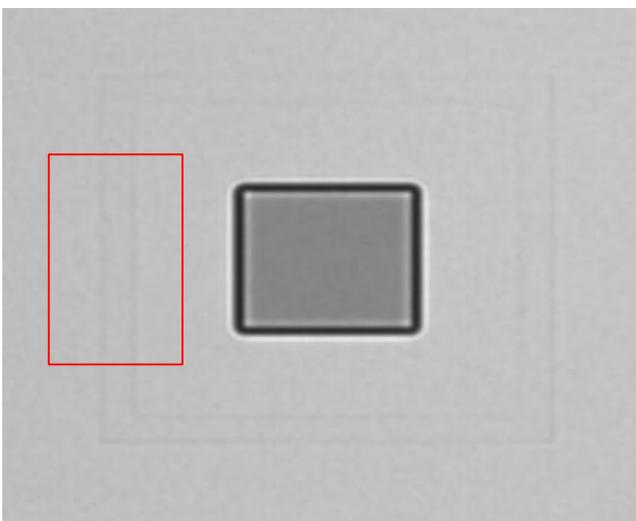


Figure 5. Low contrast box in frame target

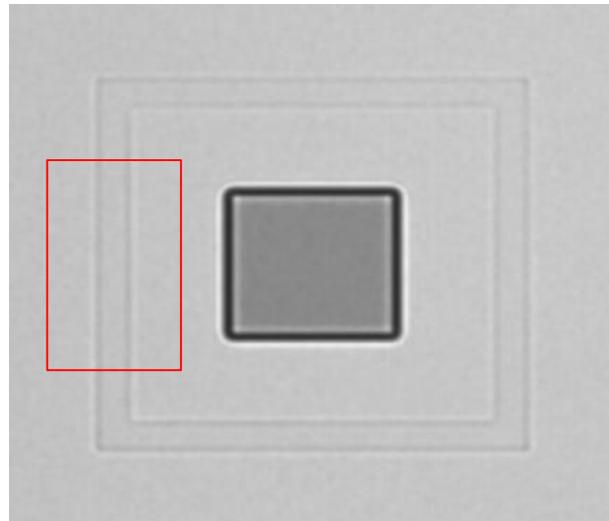


Figure 6. Higher contrast box in frame target

You can see the differences in cross-sections provided below:

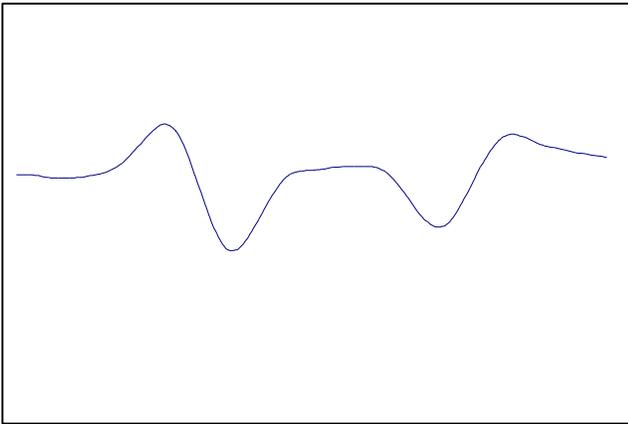


Figure 7. Figure 5 profile from boxed area

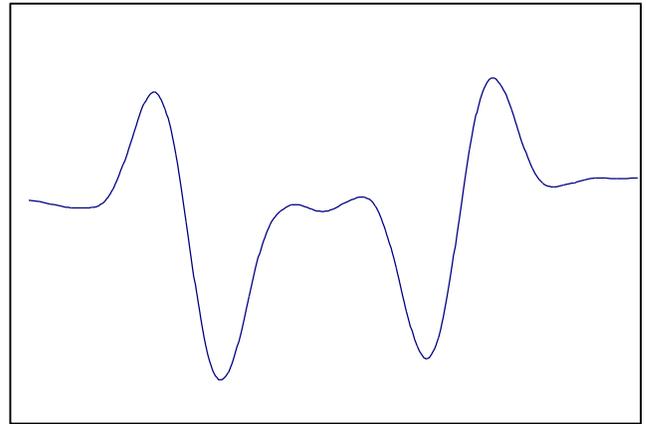


Figure 8. Figure 6 profile from boxed area

5. ALGORITHM DEVELOPMENT

Current algorithms rely on consistent edge positioning, polarity, contrast and detection, see Figure 9 and Figure 10 below. The STI process requires wider tolerances of all three of these conditions. The process can cause variations from device to device, lot to lot, wafer to wafer, as well as exposure field to exposure field.

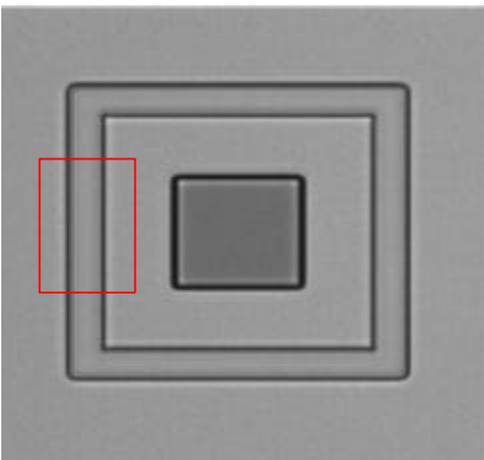


Figure 9. LOCOS Target Image

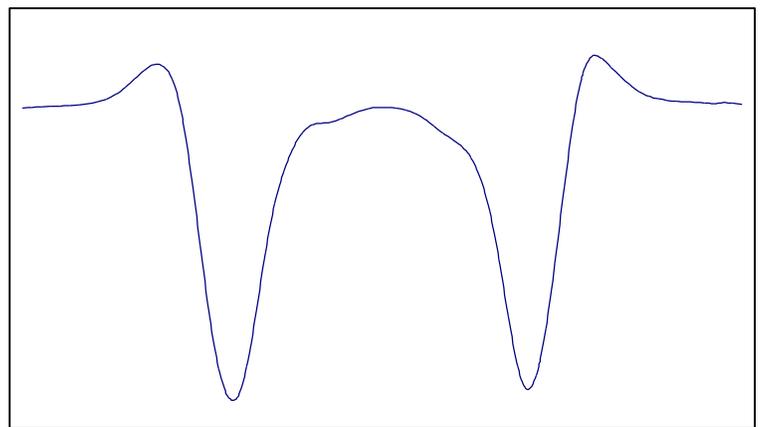


Figure 10. LOCOS Target Image profile from boxed area

A new algorithm was mandated to find the edges of the STI box in frame feature, however they appear, and consistently measure them. Granularity of the substrate must also be overcome, as it can influence edge detection. Optical filtering of the optical image enhances the edge, but can also enhance the prominence of granularity. The algorithm needs to be as robust as the standard one, but it must be more flexible in determining edges, positioning of such edges, and filtering the image without enhancing the granularity of the substrate. Most important, the algorithm needs to make measurements that are accurate.

The new algorithm considers both sides of a site simultaneously. It seeks edge structures that are present on both sides. These edges must have symmetry while having a reasonable resemblance to the predetermined edge structure in the setup. Once that kind of symmetrical structure is identified it is used to verify the center calculations of the new algorithm. This allows for significant process variation without sensitivity to that process.

The process of algorithm development is an iterative one. During initial tests, success rates indicated that the first step algorithm enhancements were working. After further testing, however, success rates, precision and accuracy would frequently change due to lot to lot variations and continuous improvement of the STI process. This led to steady improvements of the algorithm and enhanced diagnostics. As well as monitoring of systems measurements. As process conditions were tuned for improved device performance, the algorithm parameters needed to be more flexible to accommodate the changes. Finally, testing on production wafers with changes in process flows and variations from lot to lot verified that the modifications in the algorithm made the metrology tool process capable for STI. This development process required that the engineers at Micron and Schlumberger work together as a team. All data was shared, good and bad, to attain the required goals.

6. EXPERIMENTAL DATA

All data was taken using a variety of wafers. Test wafers as well as production wafers were included. Target structures varied in structure from lot to lot, within a wafer, and sometimes within a field. Various target structures were included to insure the robustness of the algorithm. Multiple measurements were taken to rule out machine differences, wafer and lot variation. Measurements were made on all fields of the wafer. Only data from structures not present on the wafer were omitted. If sites were present the algorithm made a measurement or reported a measurement error. Diagnostics enabling algorithm edge display, and site image storage allowed operators to run wafers while diagnosis occurred off-line.

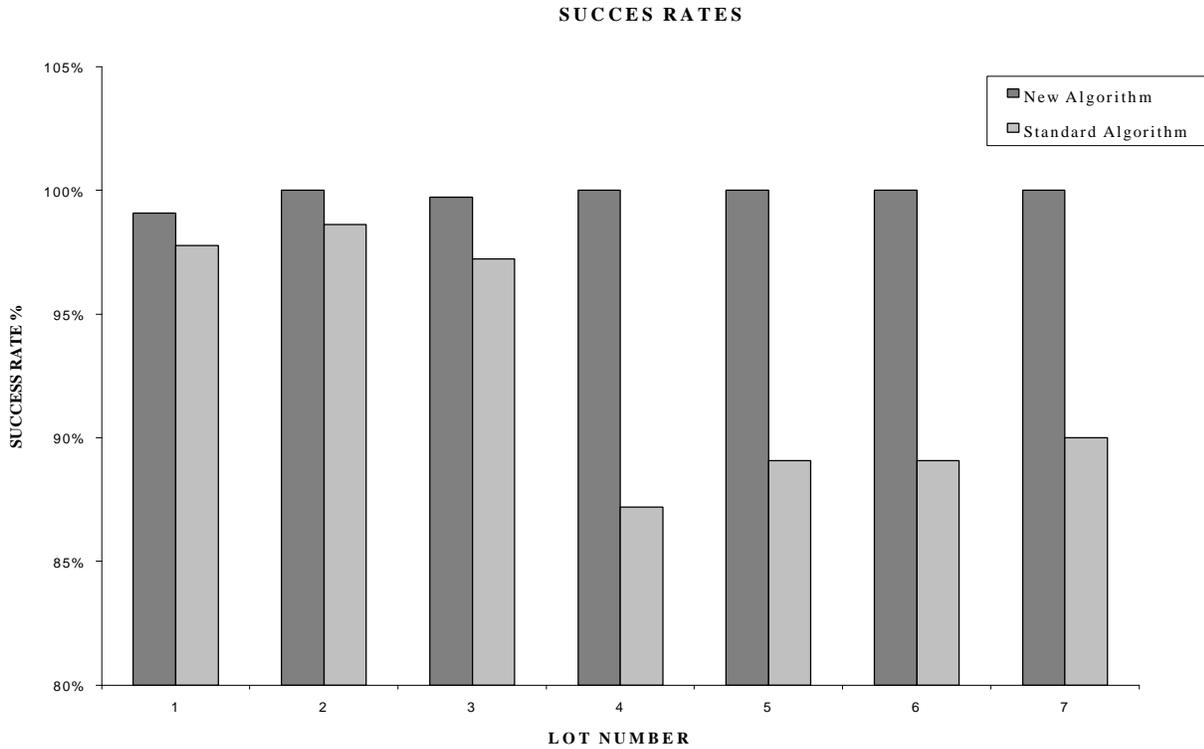
Algorithm work changed as data suggested various slopes or changes in the image profile would not accommodate production soundness. This work actually occurred at another location while production continued. Changes would then be applied via email to update necessary software files. This enabled both sides to minimize cost while not impinging upon quality of the work.

| Lot # | New Algorithm | | Standard Algorithm | | Delta | Delta |
|---------|------------------|------------------|--------------------|------------------|---------|---------|
| | X Pooled 3 Sigma | Y Pooled 3 Sigma | X Pooled 3 Sigma | Y Pooled 3 Sigma | | |
| 1 | 0.0048 | 0.0051 | 0.0060 | 0.0078 | 0.0012 | 0.0027 |
| 2 | 0.0038 | 0.0045 | 0.0058 | 0.0066 | 0.0019 | 0.0021 |
| 3 | 0.0073 | 0.0077 | 0.0057 | 0.0044 | -0.0015 | -0.0033 |
| 4 | 0.0021 | 0.0025 | 0.0055 | 0.0245 | 0.0034 | 0.0221 |
| 5 | 0.0023 | 0.0027 | 0.0091 | 0.0085 | 0.0068 | 0.0058 |
| 6 | 0.0022 | 0.0027 | 0.0101 | 0.0118 | 0.0079 | 0.0092 |
| 7 | 0.0022 | 0.0026 | 0.0083 | 0.0106 | 0.0061 | 0.0080 |
| Average | 0.0035 | 0.0039 | 0.0072 | 0.0106 | 0.0037 | 0.0067 |

Figure 11 New Algorithm vs. Standard Algorithm Data

The data given collected in Figure 11 above is representative of the hundreds of lots (multiple wafers). Measurements in X

and in Y are much more consistent relative to one another with the new algorithm. They are within angstroms, while the standard algorithm x and y precision are nanometers and tens of nanometers. The new algorithm is far superior in target edge detection at the wafer edge as well. The measurement success rate percentage is more consistent as well, see Figure 12. Variability is much more noticeable in the x and y precision of the Standard Algorithm.



| Lot # | New Algorithm | Standard Algorithm | Delta |
|----------------|---------------|--------------------|-----------|
| 1 | 99% | 98% | 1% |
| 2 | 100% | 99% | 1% |
| 3 | 100% | 97% | 3% |
| 4 | 100% | 87% | 13% |
| 5 | 100% | 89% | 11% |
| 6 | 100% | 89% | 11% |
| 7 | 100% | 90% | 10% |
| Average | 100% | 93% | 7% |

Figure 12 New Algorithm vs. Standard Algorithm Measurement Success Rates Graph and Data

7. CONCLUSIONS

Metrology of the STI process at Micron until recently has required seven costly process steps. The STI process posed a significant challenge to optics, as well as standard and proprietary measurement algorithms. The new algorithm was developed to overcome these challenges and retain competitive superiority.

With this algorithm Micron was enabled to place the STI metrology process in production and improve upon it. The data enclosed shows that the measurement of the STI process meets Micron's tolerance requirements. Seven process steps were saved that cost Micron machine time, capacity, WIP time, and engineering time. All of this amounted to a significant amount of dollars saved, which received significant attention from senior management (Micron and Schlumberger) to fund this presentation.

8. ACKNOWLEDGMENTS

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